

IGBT Behavior under Short Circuit and Fault Protection

Using Two-Step-Soft-Turn-Off Gate Driver

In inverter driven UPS or motor applications, the IGBT can be destroyed when it is turned-on into a faulted motor or an output short circuit or an input bus voltage shoot through. Under these conditions current through the IGBT increases rapidly until it saturates. After fault detection, depending on the point at which the fast turn-off pulse is applied, very different levels of hole current can flow under the n^+ source region, making this an important factor in the successful containment of the fault current. We present experimental observations showing that IGBT failure under short-circuit conditions is dependent on where and how the turn-off pulse is applied. A two-step (two-level) turn-off gate driver circuit is introduced which safely turns-off even a high transconductance IGBT during short-circuit and abnormal over current faults. This turn-off process starts during faulted condition only.

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It is very common that an IGBT used for motor drive, UPS and some other industrial applications, be selected for 10 micro-second short-circuit withstand time (SCWT) if regular de-sat protection driver is used. But this driver generates high turn-off stress to the IGBT during inverter short circuit or the output becomes faulty. Under these abnormal conditions when the IGBT is turned-off abruptly, failures can occur if the IGBT is not selected properly. If the smart fault protection is not used, high turn-off loss will be generated and even short circuit current can ramp-up to a dangerous level destroying the IGBT. There are several ways to turn-off the IGBT once fault condition is detected. Some of these are as follows:

Gate is discharged through high gate resistance. This discharge path is activated only during the above said abnormal conditions. This is not the best solution.

Gate voltage is abruptly reduced to zero.

Adding some source inductance which is common for both gate discharge path and load current. Gate de-bias occurs. But during normal condition switching loss is increased.

Sense IGBT can also be used where fault current is sensed by pilot cell but the current sense accuracy of these pilot cells is not good which is further is affected by temperature.

Gate voltage pattern analyzer for short-circuit protection in IGBT inverters [1]. These circuits are very sensitive to load changes and type of loads.

Current sense resistor or Hall-effect devices are also used to detect fault through IGBT. But again these methods either generate power loss or are costly.

But de-sat protection is the most commonly used for short-circuit and over current fault protection. De-sat detection truly provides the state of electrical over stress of IGBT under current fault condition when gate voltage is high. Reducing gate voltage in a controlled manner to just above gate threshold voltage is preferred and described in this article. This will reduce fault current and after some finite time gate voltage is brought down to zero safely, turning-off the IGBT without stress.

Gate Drive Circuit

The main function of any gate driver circuit is to convert a control signal to a power signal that can efficiently controls the IGBT or MOSFET turn-on and turn-off. If the IGBT or MOSFET requires short circuit protection, the gate drive circuit must safely turn-off the switch during a shorted or abnormal overload condition. A more detailed list of the gate drive circuit requirements for an IGBT or MOSFET are as follows:

A controlled turn-on and turn-off of the IGBT so as to optimize the conduction and switching losses.

In some applications, electrical isolation between control circuit and power circuit is very important.

In the case of a short circuit condition, the IGBT should be protected and turned-off safely with minimum power dissipation and stress. The gate drive circuit should be able to minimize short circuit current and short-circuit withstand time without device failure. If both of these parameters are minimized, the power dissipation under short circuit will reduce and the system reliability will increase.

During a short circuit condition, the IGBT collector to emitter voltage can rise fast. The voltage across the gate to emitter should not be

allowed to rise due to gate to collector displacement current flowing into the gate to emitter capacitance, C_{ge} . Current flowing into C_{ge} will cause V_{ge} to rise and further increase the short circuit current. One should make sure that this condition is avoided.

Preferably a totem pole output stage with separate turn-on and turn-off resistance option. The gate discharging switch of the totem pole should be as close as possible to IGBT and minimize the loop inductance between this switch and IGBT gate & emitter terminals.

Minimize the propagation delay time between input and output pulses of the gate driver.

De-Saturation

The de-saturation detection technique for identifying a short circuit and fault condition in an IGBT is well known. Generally, a de-saturation condition is said to exist if the voltage across the IGBT collector to emitter terminals rises above 5-8 volts while the gate to emitter voltage is high. This condition indicates that the current through the IGBT has exceeded the normal operating level. The gate drive circuit should be designed so that it reacts promptly to the short circuit and safely turns-off the IGBT within SCWT rating of the IGBT. However, in recent years, IGBTs have been designed with lower conduction and switching losses but this generally reduces SCWT. IGBT technology utilizes shallow junctions to decrease switching and conduction losses. However these new technologies have increased the transconductance (g_m) of the IGBT. Since the magnitude of the IGBT short circuit current is directly proportional to g_m , during a short-circuit condition, a higher collector current results. The large collector current and high bus voltage place the IGBT in a state of high instantaneous power dissipation that can only be sustained for a few microseconds. The gate drive circuit must respond very quickly and efficiently to the fault current to protect the IGBT. Due to the two-step turn-off, the IGBT with even 4 microseconds short circuit withstand time can safely be turned-off and protected. The IGBT, used in conjunction with the two-step turn-off gate drive, safely turns off low impedance over-current faults and shorted bus conditions where single-step gate drivers fail. The industry standard (10 μ s) SCWT is no longer required when the IGBT is used with this gate driver.

IGBT Behavior during short circuit and over current

The peak current during a short circuit is limited by the g_m of the IGBT. Moreover, the rate of rise of the current is limited by the turn-on characteristics of the IGBT in combination with common emitter inductance. If IGBT collector current does not saturate and reach a state of equilibrium and bus voltage has not raised high enough attempting to turn off the IGBT during can lead to IGBT latch-up [2]. In case of fault conditions very different hole current flow under n^+ source regions. These different hole current conditions and patterns of hole current under n^+ source generate different electrical stress. In case if the gate voltage is brought down abruptly to zero before the device voltage reaches clamp, the IGBT can latch-up and fail. Flow of electron through the channel is cutoff once the gate is turned off. Holes continue to inject from emitter of p-n-p structure which is known as IGBT collector. This process stops when electrons in IGBT N-base are depleted. At this point IGBT current is almost all hole current. The amount of holes is very high here and if IGBT does not reach clamp voltage IGBT can latch-up and fail. However if enough time is allowed to complete this process and plasma of electrons in IGBT N-base is reduced or depleted so that base current reaches zero. At this point the carriers from emitter of IGBT p-n-p transistor are no longer injected and IGBT current is almost all hole current. IGBT voltage rises at a rate so that edge of the depletion spread can

sweep out enough carriers to maintain inductive current. If enough time is allowed to stabilize the bus voltage while the channel current is flowing, the IGBT N-base is depleted and because of this current flow is more uniformly distributed. The displacement current becomes very small since dv/dt reduces and latch-up is avoided. If enough time is not allowed for the IGBT to reach clamp voltage and gate voltage is removed abruptly, IGBT voltage will rise with high dv/dt and current in IGBT is non-uniformly distributed, high displacement current generated by high dv/dt can latch-up IGBT. Non-uniform gate ESR combined with Miller capacitance result in non-uniform turn-off of IGBT active area. This results into high localized hole current density flowing laterally in P-base of parasitic n-p-n bipolar resulting in latch-up of parasitic thyristor. Because of these reasons one has to wait until IGBT reaches clamp voltage collector current saturates. So it is safer to choose IGBT with 10 microseconds SCWT for motor drive and UPS inverter applications if a regular gate driver is used.

Two step soft turn-off gate drive

It is clear that if the collector to emitter voltage rises to the DC Bus slowly and high transconductance increases short circuit current, regular driver does not protect an IGBT with a low short circuit withstand time (<5 μ s). However the longer SCWT comes at the cost of higher switching and conduction losses. The rate of rise of the collector to emitter voltage is dependent upon the operating conditions and can take several microseconds to rise to bus voltage. However, the gate drive must respond quickly to initiate turn off to protect a low SCWT IGBT. The only solution is to lower the gate voltage to just above threshold voltage of the IGBT. The IGBT reaches clamp voltage faster and reduces IGBT current during fault.

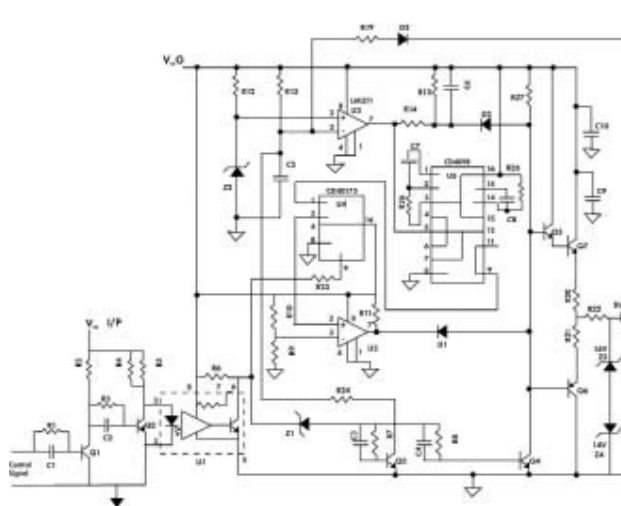


Figure 1: Two-step gate drive circuit

The schematic of two step gate driver is shown in Figure 1. The gate driver output will produce a positive signal with respect to the IGBT emitter terminal when the control signal goes high. As the control signal goes high, transistor Q1 turns on, Q2 turns off, and the LED of optocoupler U1 turns on. This forces the output voltage of the optocoupler to the low state. When the optocoupler output goes low, both transistors Q3 and Q4 turn off, turning on the Darlington combination of transistors Q5 and Q7. This will connect the V_{on} supply to the gate of the IGBT through the gate turn-on resistor initiating the IGBT turn-on process.

During the time that transistor Q4 is off, the output stage PNP transistor Q6 remains off. Once the IGBT is turned on, the inverting input

of comparator U3 will be clamped to one diode drop (forward voltage drop of de-saturation diode DC) plus the IGBT V_{cesat} voltage. For the gate driver to operate properly, the inverting voltage node must be at a lower voltage level than the non-inverting voltage node. The non-inverting input voltage is set by zener diode Z2. When the control signal goes low, the LED of U1 turns off, and the optocoupler output voltage V_{on} goes high with respect to negative terminal of V_{ccG} . This turns on transistors Q3 and Q4. When Q3 turns on, capacitor C5 discharges through R24 allowing the output of the comparator U3 to remain high. Once transistor Q4 is on, the output stage Darlington combination turns off, and the PNP transistor Q6 turns on. Now, the gate of the IGBT will discharge through R21, R22 and transistor Q6, initiating the IGBT turn-off. During normal operation (no short-circuit or overload condition) comparator U3 remains off without effecting the gate driver circuit.

However, the de-saturation circuit activates when a fault occurs at the inverter output, or the complimentary IGBT turns on due to noise. When the IGBT is turned-on into the low impedance load, it draws a large current, which causes the collector to emitter voltage of the IGBT to rise towards the bus voltage. As the IGBT collector to emitter voltage rises, the voltage across capacitor C5 will begin to charge towards V_{ccG} .

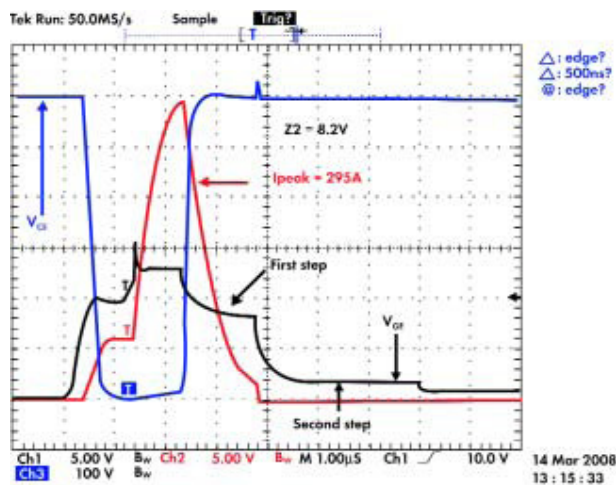


Figure 2: Trench IGBT (FGA25N120ANTD) into short circuit 'case 1'

When the voltage across C5 rises above Z2 zener voltage, the comparator U3 turns-on. When U3 turns on, the base voltage of Darlington transistor Q5 lowers to approximately 8 volts with some quick slope. R14, R15, R27, C6 and D2 set this voltage and slope. The applied gate voltage of the IGBT is reduced from approximately 13 volts to about 8 volts, significantly decreasing the saturation current of the IGBT. As soon as the gate bias reduces, electron current (MOSFET current) reduces. As electron current reduces, base current of the IGBT structure PNP transistor reduces. Hence, the saturation current of the IGBT reduces.

When IGBT is turned-on into an inductive short-circuit or it is under shoot through condition current ramps quickly. The voltage across the device increases and current through the IGBT saturates if the gate voltage is kept on. Now if the gate voltage is brought to zero after IGBT current saturates and drain voltage rises to clamp voltage the IGBT will turn-off safely.

The I_c U4 & U5 decide the time duration of first step level voltage and after this time the comparator U2 turns on and transistor Q5 &

Q7 turn-off and Q6 turns-on turning-off IGBT safely. During first step time, the collector to emitter voltage across the IGBT rises faster than it would by holding the gate at 15 volts. As previously mentioned, the faster collector to emitter voltage rise is beneficial for the IGBT to safely turn-off the IGBT under a shorted load.

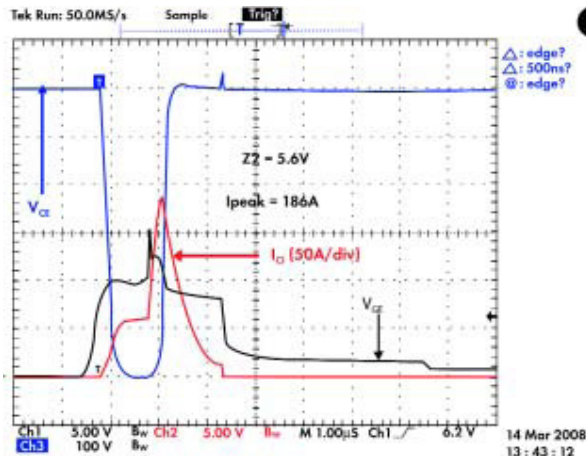


Figure 3: Trench IGBT (FGA25N120ANTD) into short circuit 'case 2'

Figure 2 and Figure 3 depicts the Fairchild 1200V Trench IGBT turning on into a resistive load and after 1 micro-second the resistor is shorted. In 'case 1' IGBT is protected within 2.6 micro-seconds. The zener Z2 decides when to start first step. The second step voltage level is decided by D1 and V_{be} of gate turn-on transistor as shown in figure 2. When the zener Z2 value is 8.2V, that allows IGBT peak current to rise up to about 300A but still it turns-off IGBT safely as shown figure 2 'case 1'. But in figure 3 'case 2' when this zener value is reduced to 5.6 volts the short circuit current only rises up to about 190A. By selecting this zener properly depending on type of IGBT technology one can reduce this short circuit peak current and increase system reliability.

Summary

A new two-step gate drive circuit has been proposed which protects the IGBT during short circuit and over load fault. The gate-drive safely turns-off the IGBT in two steps. The IGBT stress during short circuit or fault current conditions is minimized. The new gate drive circuit can safely shut-off IGBTs with SCWT as low as 3 μ sec. The Fairchild trench IGBT can be turned-off safely in less than 3 micro-seconds.

REFERENCES

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